ABSTRACT OF THE DISCLOSURE

The invention incorporates a signal processing circuit having a data input-output (I/O) circuit, a microprocessor, a dedicated processing circuit, a local memory, and a memory access control circuit interconnected over a bus. The bus includes a system bus and a local memory bus. The system bus connects to the data I/O circuit, microprocessor, dedicated processing circuit, and memory access control circuit. The local memory bus connects to the local memory. First, second, and third connection circuits connect between the system bus and local memory bus, between a first local bus in the dedicated processing circuit and the local memory bus, and between a second local bus in the data I/O circuit and the local memory bus. The memory access control circuit controls the first, second, and third connection circuits according to priorities assigned for the connection circuits. The system bus transfers control information among the data I/O circuit, dedicated processing circuit, and memory access control. If the data I/O circuit, dedicated processing circuit, and microprocessor request data transfers to or from the local memory, the data I/O circuit, dedicated processing circuit, and microprocessor each issues a local memory bus use request to the memory access control circuit. The memory access control circuit then determines which of the second local bus, first local bus, and system bus will be connected to the local memory bus, while the other buses are disconnected therefrom. Thus, the data I/O circuit, dedicated processing circuit, and microprocessor are able to act independently of one another.